PCI-SIG DEVELOPERS CONFERENCE 2017

PCI-SIG® DEVELOPERS CONFERENCE 2017

June 7-8

SANTA CLARA CONVENTION CENTER
Santa Clara, California

YOU ARE INVITED

Come Celebrate PCI-SIG® Technology!

PCI-SIG 25TH ANNIVERSARY PARTY

Wednesday, June 7 | 5:30-8:00 PM

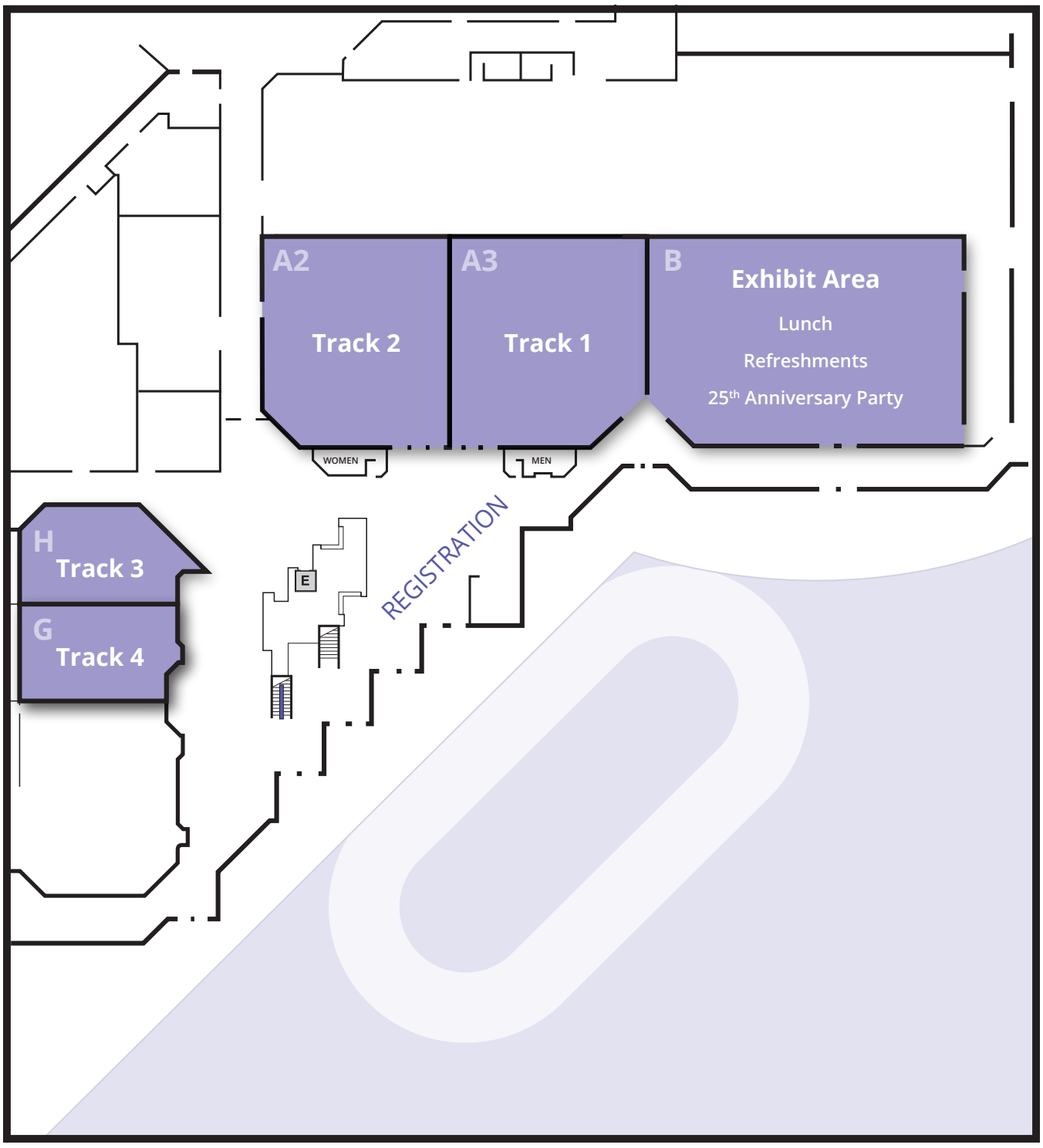
Please join us in the Sponsor Exhibit Area for appetizers and refreshments at 5:30 p.m. This will be a great opportunity for some informal Q&A, networking, and time to mingle with speakers, sponsors, and other attendees. The Sponsor Exhibit Area showcases industry-leading member companies and their most recent product developments and designs based on PCI architectures and tools.

We will also be hosting a Trivia Night-themed dinner, so we'd recommend using this time to mingle with our Sponsors--who will be distributing clues--and gather key intel ahead of the game. Clues you earn during this portion of the evening will assist your team in answering the trivia questions to follow. The winning team will be dubbed PCI-SIG Trivia Champions and walk away with top-notch prizes in-hand!

The Trivia Night-themed dinner will kick-off promptly at 7:00 p.m. and test attendees' knowledge of the ins and outs of PCI technology. We ask that you select your dinner party wisely as each table round will be considered a team. You won't want to miss this memorable event!

PCI-SIG DEVELOPERS CONFERENCE 2017

FLOOR PLAN



PCI-SIG DEVELOPERS CONFERENCE 2017 | Agenda

DAY 1 – JUNE 7TH		TRACK 1 – PCI EXPRESS®	TRACK 2 – PCI-SIG ARCHITECTURE
8:00 – 9:00	Foyer	Registration in Foyer	
9:00 – 9:30		Introductory Keynote / Annual Members Meeting	
9:30 – 10:30	Session 1	PCIe® 4.0 Electrical Update	PCI-SIG Architecture Overview
10:30 – 11:30	Session 2	PCIe CEM 4.0 Previews	PCIe Cable Update
11:30 – 1:00	Exhibit Area	Lunch and Exhibit	
1:00 – 2:00	Session 3	PCIe 4.0 PHY Logical	PCI Express Basics
2:00 – 3:00	Session 4	PCIe Compliance Updates	PCIe Electrical Basics
3:00 – 3:30	Exhibit Area	PM Break and Exhibit	
3:30 – 4:30	Session 5	PCIe 4.0 Protocol Update	M.2 Updates
4:30 – 5:30	Session 6	PCIe Panel Discussion	
5:30 – 8:00	Exhibit Area	PCI-SIG 25th Anniversary Party	

DAY 2 – JUNE 8TH		TRACK 1 – PCI EXPRESS	TRACK 2 – PCI-SIG ARCHITECTURE
9:00 – 10:00	Session 7	PCIe 4.0 Electrical Update	PCI-SIG Architecture Overview
10:00 – 10:30	Exhibit Area	AM Break and Exhibit	
10:30 – 11:30	Session 8	PCIe CEM 4.0 Previews	PCIe Cable Update
11:30 – 12:30	Session 9	PCIe 4.0 PHY Logical	PCI Express Basics
12:30 – 1:30	Exhibit Area	Lunch and Exhibit	
1:30 – 2:30	Session 10	PCIe Compliance Updates	PCIe Electrical Basics
2:30 – 3:30	Session 11	PCIe 4.0 Protocol Update	M.2 Updates

TRACK 3 – MEMBERS IMPLEMENTATION	TRACK 4 – MEMBERS IMPLEMENTATION
Registration in Foyer	
Introductory Keynote / Annual Members Meeting	
PCIe Error Detection and Recovery Mechanisms	Challenges and Techniques for Implementing Lane Margining
PCI Express in Automotive Infotainment and ADAS Processors	PCI Express Link Training and Protocol Debug Techniques
Lunch and Exhibit	
Refclk Fanout Best Practices for 8GT/s and 16GT/s Systems	Jitter Measurements in the 0.7 4.0 PCI Express Base Specification
In-system Debugging of PCIe Devices	
PM Break and Exhibit	
Performance Tuning PCIe Systems	
PCIe Panel Discussion	
PCI-SIG 25th Anniversary Party	

TRACK 3 – MEMBERS IMPLEMENTATION
Demystifying the PCIe Plug-Unplug
AM Break and Exhibit
Lessons Learned Bringing Up Early Adopter PCIe 4.0 Links
Multi-DMA Virtualization within Virtualized PCIe Systems
Lunch and Exhibit
New Challenges in Compliance Test and Debug for PCIe 16GT/s
Verification Challenges for Retimers

PCI-SIG DEVELOPERS CONFERENCE 2017 | Presentation Abstracts

PCI EXPRESS® | TRACK 1

PCIe 4.0 Electrical Update
Track 1: Session 1, Session 7
Presenter: Dan Froelich

In transitioning to PCIe 4.0 the raw data rate is being doubled to 16GT/s keeping the same efficient encoding used for the PCIe 3.0 8GT/s data rate. The PCIe 4.0 Base Specification divides up the electrical layer into four components: Transmitter, Channel, Receiver and Reference Clock. The PCIe 4.0 preliminary specification for each component will be discussed along with the rationale behind the parameters specified and the measurement methodologies and potential updates to methodologies under discussion for PCIe 4.0. This session is geared toward experienced PCI Express PHY designers and validation engineers.

PCIe CEM 4.0 Previews
Track 1: Session 2, Session 8
Presenter: Dan Froelich

This presentation provides updates on the recent PCI Express specification development work in the PCI-SIG Electromechanical Workgroup. The presentation focuses on providing an overview of the preliminary PCI Express Card Electromechanical Specification 4.0 (CEM 4.0) and provides an overview of several potential improvements under investigation to improve the CEM connector to support 16GT/s signaling while maintaining backwards compatibility.

PCIe 4.0 PHY Logical
Track 1: Session 3, Session 9
Presenter: Debendra Das Sharma

This session will cover important aspects of the PCIe 4.0 Logical PHY specification as it is being developed. The talk will focus on the PCIe 4.0 encoding, Tx equalization, enhancements to the per-Lane error logging mechanism to work with retimers, Ordered Set changes to meet the PCIe 4.0 Data Rate, compliance pattern, and Lane Margining at Receiver. People who are designing, validating, or specifying the latest generation of PCIe components are the target audience for this session.

PCIe Compliance Updates
Track 1: Session 4, Session 10
Presenter: David Bouse

This presentation outlines the requirements for PCI Express compliance and interoperability. It provides an overview of all testing performed for the PCIe 3.x and PCIe 2.x compliance programs—with a focus on updates/changes for the 3.x program and first look at PCIe 4.0. Every component of the PCIe compliance program is discussed including electrical, protocol, platform BIOS, and configuration testing. This session will also cover the timeline for upcoming Compliance Workshop events worldwide, where members can validate their parts for compliance to the PCI-SIG "Gold" suite of tests.

PCIe 4.0 Protocol Update
Track 1: Session 5, Session 11
Presenter: Joe Cowan

This session covers PCI Express protocol changes over the last two years or so, including completed ECNs, selected ECRs under development, and major changes developed for PCIe 4.0. Completed ECNs include Emergency Power Reduction with PWRBRK Signal, RC Integrated Endpoint & IOV Updates, Expanded Resizable BARs, Extended Message Data for MSI, SR-IOV Table Updates, VF Resizable BARs, Flattening Portal Bridge (FPB), and Hierarchy ID Message. Selected ECRs under development include Firmware Validation and Native PCIe Enclosure Management (NPEM). Major PCIe 4.0 protocol changes involve 10-Bit Tags, Scaled Flow Control, simplified protocol timers, and the incorporation of other PCI specifications into the PCIe Base Specification.

PCI-SIG ARCHITECTURE | TRACK 2

PCI-SIG Architecture Overview
Track 2: Session 1, Session 7
Presenter: Richard Solomon

This presentation will provide an overview of PCI™, PCI-X™, and PCI Express. Basic protocol details, and key concepts such as Configuration Space, Message Signaled Interrupts, Transaction Attributes and Split Transactions which span the spectrum from Conventional PCI through PCI-X to PCI Express are explained. This presentation should be a particularly useful starting point for attendees new to PCI-SIG technologies.

PCIe Cable Update
Track 2: Session 2, Session 8
Presenters: Lee Mohrmann & Alex Haser

Learn about updates to the PCIe External Cabling and OCuLink specifications.

PCI Express Basics
Track 2: Session 3, Session 9
Presenter: Richard Solomon

In this session, attendees will learn the basics of the PCI Express Architecture. This presentation will cover the key features of PCI Express and provide an overview of the Electrical, Packet-Based Protocol and Configuration Mechanism of this high performance serial bus architecture. This session is geared towards attendees new to PCI Express technologies.

PCIe Electrical Basics
Track 2: Session 4, Session 10
Presenter: Dean Gonzales

This session will give an overview of the electrical signaling and features for 2.5GT/s, 5GT/s and 8GT/s along with a description of the target channels that are used as the basis for the electrical specification definition. The key electrical characteristics of the transmitter, receiver and reference clock will be described along with interpretation of their relevance to system applications. This session is geared towards attendees wanting an introduction to the electrical concepts behind PCI Express technologies.

M.2 Updates
Track 2: Session 5, Session 11
Presenter: Manisha Nilange

M.2 specification is currently at Rev 1.1. (Published on Dec 15, 2016). 12 ECNs were incorporated post Rev 1.0 specification release. The presentation is aimed at giving a snapshot of the changes that went into the specification Rev 1.1. The presentation will also walk through the changes incorporated into the latest Mini CEM Specification Rev 2.1 (Published on Dec 15, 2016). In addition, part of the presentation will cover the movement into smaller storage devices by showing the current and upcoming BGA form factors. This presentation will also show the 16x20mm and 11.5x13mm packages along with the advantages and challenges to support these devices in the platform.

MEMBERS IMPLEMENTATION | TRACK 3

PCIe Error Detection and Recovery Mechanisms
Track 3: Session 1
Presenter: Gord Caruk

Streams of TLPs, DLLPs, and Ordered Sets will be exhaustively examined to demonstrate that PCI Express handles any single bit error (and many more significant errors). This presentation will show which PCIe features are used in detecting those errors and in recovering from them. Attendees will learn the value of the various CRC, parity, sequence number, retry, etc. mechanisms, and why they are necessary elements of the PCI Express specification.

PCI Express in Automotive Infotainment and ADAS Processors
Track 3: Session 2
Presenter: Brad Cobb

PCI Express plays an important role in the design of embedded Automotive Infotainment and ADAS systems. It enables scalable system architectures via high-speed co-processor communications and provides connectivity via the latest wireless standards. There are, however, many challenges and nuances related to implementing PCI Express into embedded automotive processors. These span from unique architectural requirements to validation and support challenges. This presentation will highlight several examples of these challenges including: Processor integration, SerDes sharing/multiplexing, Functional Safety, automotive validation, and customer documentation.

Refclk Fanout Best Practices for 8GT/s and 16GT/s Systems
Track 3: Session 3
Presenter: Greg Richmond

As PCIe data rates increase from 8GT/s to 16GT/s and beyond, the system Refclk quality at the load must improve. This requires increased attention to clock fanout architecture, routing, and measurement accuracy. This presentation will cover the theory and experimental validation of various clock fanout architectures (single source to multiple cascaded buffers), routing (up to 60 inches with and without aggressors), and measurement accuracy (including compensation of sampling scope noise floors) to ensure compliance at 8GT/s and 16GT/s. Clock placement effects on signal integrity and jitter transfer functions will also be highlighted, allowing designers to maximize the data eye opening.

In-system Debugging of PCIe Devices
Track 3: Session 4
Presenter: Philippe Legros

Even with proper validation it is not uncommon that a PCI Express device does not behave as expected in hardware. There can be so many reasons for a link training issue or a link instability issue that engineers are then facing the difficult and time consuming challenge of finding the root cause(s) of the improper behavior. This presentation will go through the problems that are the most commonly encountered in hardware, and which techniques and tools are the most appropriate to isolate and troubleshoot each of them.

Performance Tuning PCIe Systems
Track 3: Session 5
Presenter: Paul Cassidy

The PCI Express Base Specification includes options for a wide variety of performance-related parameters, but how is a designer to know the optimum settings for a given environment? This presentation covers several key features – including maximum payload size, number of outstanding transactions (tags), maximum read request size, etc. Using simulations against an off-the-shelf PCIe controller, the performance benefits and size/area "costs" of various settings for these features will be shown. Guidance will also be given around practical limitations with real-world systems. This session should be of interest to anyone designing or configuring PCI Express interfaces to meet particular performance goals.

Demystifying the PCIe Plug-Unplug
Track 3: Session 7
Presenter: Alex Umansky

The Hot Plug and Unplug of PCIe devices has always presented a major challenge for silicon, systems and software developers. The rapidly growing popularity of PCIe SSDs in Data Centers gives rise to the need for effective solutions allowing a surprising disconnect of devices, without system crashes and performance degradation. The presentation explorers several plug and unplug hardware detection methods including the procedures described in the specification and also some best practices that de-facto became industry "standards". Plug-unplug software techniques are described along with discussions on timing and resources allocation restrictions. Recent changes to the specification and related configuration capabilities are covered. And finally, the presentation is a call for further discussions by the committee members.

Lessons Learned Bringing Up Early Adopter PCIe 4.0 Links

Track 3: Session 8

Presenter: Richard Solomon

This presentation covers pitfalls found trying to interoperate early adopter designs supporting 0.5 and 0.7 drafts of the PCIe 4.0 specification. Initial link bringups are always challenging, and mixing pre-release devices adds further complexity. The presentation will show design for debug features that can be incorporated to assist, as well as methods for using standard test tools and PCIe-specific knowledge to determine WHY a link is not coming up, not staying up, or not negotiating the desired speed. These tools and techniques will also provide valuable insight for first adopters who will be integrating final PCIe 4.0 devices upon release.

Multi-DMA Virtualization within Virtualized PCIe Systems

Track 3: Session 9

Presenter: Stephane Hauradou

The drastically increasing amount of data to process and the ever-growing number of applications to run in today's Data Centers require optimal data transfers within virtualized PCIe systems. This presentation will discuss the specifics of virtualized DMA engines when attached to PCIe devices, as well as the technical challenges in fully supporting SR-IOV, ensuring non-blocking and concurrent operations, proposing fair arbitration between Virtual Machines, and guaranteeing Virtual Machine isolation, while achieving best performances in term of throughput and latency.

New Challenges in Compliance Test and Debug for PCIe 16GT/s

Track 3: Session 10

Presenter: Jim Dunford

As design margins shrink, accurate and standard-specific measurement is key to debugging, verifying design and performing interoperability testing when designing PCIe devices. Having confidence in test processes, workflows and results will allow you to reach compliance faster. This presentation will provide the information you need to do just that. We will discuss the most recent PCIe 3.0 and 4.0 versions and provide an in-depth look at: PCIe Transmitter (Tx) and Receiver (Rx) Compliance Testing, Current Testing Challenges and Solutions for both Tx and Rx Gen1-4, including PHY and protocol-aware testing, and Debugging Loopback Initiation and Link Training with protocol-aware BERTScope and high-bandwidth oscilloscope.

Verification Challenges for Retimers

Track 3: Session 11

Presenter: Munish Goyal

In this presentation, we propose a novel and comprehensive approach for functional verification of Retimer/Extension devices to compensate for the reduced trace lengths at PCIe 4.0 speeds. This session seeks to present a comprehensive metric driven verification (MDV) approach using coverage and checks (assertion) for verification closure of the layer using the Universal Verification methodology (UVM). We discuss a highly re-usable framework for creating an architecture for PCIe 4.0 verification which is easily scalable and can be used at module as well as SoC level.

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MEMBERS IMPLEMENTATION | TRACK 4

Challenges and Techniques for Implementing Lane Margining

Track 4: Session 1

Presenter: Gopi Krishnamurthy

Lane Margining at the Receiver is a new feature introduced in the PCIe Rev 4.0, Ver 0.7 Spec. This presentation will provide an in-depth overview of this feature and how it affects the design and integration of the PCIe Controller and PHY. We look at potential corner cases of Lane Margining Commands and how to address them in your design. This presentation also looks at how lane margining can be verified by understanding the lane margining commands between MAC and PHY. An example case study on how to use lane margining for efficient diagnostic & management of a PCI Express based system.

PCI Express Link Training and Protocol Debug Techniques

Track 4: Session 2

Presenter: Gordon Getty

PCI Express uses a layered architecture, which allows a separation of the physical interconnect from the higher level protocol. However, when debugging PCI Express problems, it is important to be able to identify which layer is causing the problem to be able to find the root cause. PCI Express 4.0 supports several new features including 16GT/s data rate support. This presents new challenges for developers during bring up and validation. This presentation will discuss techniques applicable to testing Link Training and Protocol for all PCI Express devices, including those designed to the PCI Express 4.0 Specification.

Jitter Measurements in the 0.7 4.0 PCI Express Base Specification

Track 4: Session 3

Presenter: Savitha Muthanna

The new 0.7 version of the 4.0 Base Specification specifies a number of jitter measurements. This presentation specifically discusses the implementation of the generation 1/2 UTJ, UDJDD, UPW-TJ and UPW-DJDD. The measurement methodology first determines the data dependent jitter by using regular expressions to pattern match the 8b/10b pattern, records edges in a dictionary, calculate the correlated jitter for each edge and discount it from the edge. It then goes on to construct PDFs and hash edges and finally calculates the UTJ and UDJDD. Similarly, UPW-TJ and UPW-DJDD are calculated by first calculating the Data Dependent Jitter. Section 2 discusses the implementation of Reference Clock jitter measurements for both Common Clock as well as Independent Reference Clock configurations.

PCI-SIG EVENTS 2017

PCI-SIG Compliance Workshop #102
August 1-4, 2017
Embassy Suites Silicon Valley
Milpitas, California

PCI-SIG Developers Conference Israel 2017
September 18-19, 2017
Hilton Tel Aviv
Tel Aviv, Israel

PCI-SIG Developers Conference Asia-Pacific Tour 2017
Tokyo - *October 12, 2017*
Taipei - *October 16-17, 2017*

PCI-SIG Compliance Workshop #103
October 17-20, 2017
The Westin Taipei
Taipei, Taiwan

Watch for participation opportunities on the PCI-SIG website at www.pcisig.com.

PCI-SIG DEVELOPERS CONFERENCE 2017 | Speakers

DAVID BOUSE

David Bouse graduated from PSU with a strong interest in signal integrity and digital signal processing. Currently in his fourth year at Intel, David works on Tx/Rx Test Development with a focus on Waveform Post Processing Algorithm design, fixture development, and test methodologies. David finds the numerous challenges associated with Rx Calibration and JTOL Testing of particular interest.

GORD CARUK

Gord Caruk is a Fellow Design Engineer at Advanced Micro Devices. He has >30 years of computer architecture and design experience, >20 of that at ATI/AMD, where his work has focused on I/O system interconnect. Gord has been an active contributor to the PCI-SIG for many years and is a Director on the PCI-SIG Board.

PAUL CASSIDY

Paul Cassidy is a Senior R&D Manager for Synopsys' DesignWare PCI Express Controller IP, based in Dublin, Ireland. With 20 years of industry experience, Paul has worked on the architecture and design of Synopsys PCI Express controller since joining Synopsys in 2009. Paul has a BEng from University College Cork.

BRAD COBB

Brad Cobb is a Hardware Applications Engineer at Texas Instruments, working in the Automotive Processor group. His focus is on specification, validation, and support of high-speed interfaces including PCI Express. He received his BS and MS in Electrical and Computer Engineer at Texas A&M University in 2004.

JOE COWAN

Joe Cowan is a Senior Systems Architect in Hewlett Packard Enterprise. He represents HPE in the PCIe Protocol Workgroup, where he's authored numerous ECNs and errata. During his 38-year career with HP/HPE, Joe has worked in many other areas, including InfiniBand, PCI-X, chipset design, platform architecture, OS development, and security.

DEBENDRA DAS SHARMA

Dr. Debendra Das Sharma is a Senior Principal Engineer at Intel's Data Center Group with 23 years of industry experience. He leads PCI Express, Coherency, MCP, Rack-Scale architecture, and micro-architecture. He is a leading contributor to the PCI Express specification in PCI-SIG. He has 87 patents.

JIM DUNFORD

Jim Dunford is a Product Marketing Manager in the Tektronix Performance group, specializing in Bit Error Rate products and applications. Jim came to Tektronix in early 2010 with the acquisition of SyntheSys Research, the BERTScope company, and has more than 20 years of experience with BERT applications, sales, marketing and customer support. Prior to joining SyntheSys Research, Jim held a variety of engineering, engineering management and product management positions at DRS Technologies, Ampex, and General Motors.

DAN FROELICH

Dan Froelich is a staff engineer/architect at Intel Corporation. He received a BS in Physics from Harvey Mudd College in 1996. Dan played key roles in the technical planning and compliance method and tool development for the USB 2.0, PCIe 1.1 and 2.0, Wireless USB and WiMedia compliance programs. He also authored portions of the PCIe 2.0 CEM, Wireless USB, USB 3.0, and WiMedia technical specifications. Dan currently chairs the PCI-SIG CEM Workgroup and Co-Chairs the PCI-SIG Electrical Workgroup in addition to the Serial Enabling Group which is now working on the PCI Express 4.0 Compliance Program.

GORDON GETTY

Gordon Getty is a Senior Application Engineer at Teledyne LeCroy. He has been working on PCI, PCI-X and PCI Express technologies for over 15 years. He has developed many test procedures for testing PCI Express devices including some used by the PCI-SIG for compliance testing. Gordon is also an active contributor to the PCI Express Link Transaction and BIOS test specifications for both PCI Express 2.0, 3.0 and 4.0 testing. Gordon graduated from Glasgow University in Scotland with a Bachelor's degree in Electronics and Music and a Master of Science in Information Technology from the University of Paisley in Scotland.

DEAN GONZALES

Dean Gonzales is a member of the PHY design team at AMD and is involved with circuit architecture analysis, channel modeling, and signal integrity simulation. Prior to joining AMD, Dean worked at Broadcom and Intel and has over 18 years of experience with high-speed hardware development, package design, and semiconductor circuit design.

MUNISH GOYAL

Munish works as Principal Product Engineer at Cadence Design Systems leading the Product Engineering team for PCIe Verification IP at Cadence. He joined Cadence in October, 2011 and since then he has worked on multiple serial interface verification IPs such as USB and Ethernet. Prior to joining Cadence, he was worked at Qualcomm and Freescale where his primary duties involved System level verification and post silicon validation of ARM core subsystem and various peripherals like MIPI CSI, DiGRF, DSI, and high performance DMAs.

ALEX HASER

Alexandra Haser is a Senior Industry Standards Engineer at Molex and Chairman of the OCuLink Workgroup. After joining Molex in 2014, she worked as a Signal Integrity Engineer and continues to focus on the performance of high speed I/O interconnects. Alex earned her B.S. and M.S. degrees in Industrial and Enterprise Systems Engineering from University of Illinois, Urbana-Champaign.

STEPHANE HAURADOU

Stephane Hauradou is cofounder of PLDA, a leading supplier of PCI Express Controller IP founded in 1996. Over the past 20 years, Mr. Hauradou has had many responsibilities in engineering and marketing, developing PLDA's first PCI controller IP in 1997, and overseeing the transition to PCI-X and PCI Express. Mr. Hauradou serves as a company Officer and Vice President, advising on corporate strategy and working day to day on corporate marketing, product marketing, and marcom.

GOPI KRISHNAMURTHY

Gopi Krishnamurthy is an Architect in the Digital IP group at Cadence Design Systems, Inc. Bangalore where he has worked on PCIe IP since 2014. He currently involved in developing next generation Cadence IP for PCI Express applications. Previously he has worked for Lattice and Altera as engineering team lead, focused in developing PCI Express Controller IP's for FPGA's. He received his BSEE from University of Mysore India in 1992. He currently holds 4 US patents.

PHILIPPE LEGROS

Philippe Legros is the PCI Express design manager of PLDA Inc. In the past fifteen years he has worked on the development of PCI, PCI-X and PCI Express IP cores and he is well aware of system integration and performance issues. He is responsible for defining architecture and leading development of PCI Express based IP cores and custom solutions. He has an MSc from Middlesex University, London UK.

LEE MOHRMANN

Lee currently works in high-speed systems architecture and design at National Instruments focusing on instrumentation systems and controllers. Previously, Lee held signal integrity and systems engineering positions at Dell, Inc. developing server, desktop, and notebook platforms. Lee has a BSEE from Texas A&M University.

SAVITHA MUTHANNA

Savitha Muthanna got her B.E. in C.S. from Bangalore University and M.S. in C.S. from the University of Texas at Dallas. She worked at Agilent Technologies, Spokane, developing a multi-protocol wireless base station emulator. A strong contributor to Digital Signal Processing algorithms at Tektronix, Bangalore, she is self-taught in Electrical Engineering and Digital Signal Processing. She has contributed to the research of new standards and technologies, and undertaken feasibility studies. Her interests outside of work are Consciousness studies, epistemology, mathematics and visual art.

MANISHA NILANGE

Manisha Nilange is an I/O Architect, focusing on electrical compliance and enabling. She led development of PCIe 2.0 and 3.0 compliance test fixtures and subsequent industry enabling. Manisha has been with Intel Corporation since receiving her MS in Electrical Engineering from the University of Texas, Arlington.

GREG RICHMOND

Greg Richmond is the Director of Engineering for the Silicon Labs Timing Division. He has served as V.P. of Engineering for the timing product lines at ICS (now IDT), IMI, and Cypress Semiconductor. He has 20 patents issued in the area of integrated timing circuits and holds an MSEE from Stanford University and BSEE from Walla Walla University.

RICHARD SOLOMON

Richard Solomon is the Technical Marketing Manager for Synopsys' DesignWare PCI Express Controller IP. He has been involved in the development of PCI chips dating back to the NCR 53C810 and pre-1.0 versions of the PCI spec. Richard architected and led the development of the PCI Express and PCI-X interface cores used in an industry-leading line of storage RAID controller chips. He has served on the PCI-SIG Board of Directors for over 10 years, and continues to represent Synopsys on wide variety of PCI workgroups. Richard holds a B.S.E.E. from Rice University and 26 US Patents, many of which relate to PCI technology.

ALEX UMANSKY

Alex Umansky is a Chief Architect at Huawei, IT Product Line, where he defines PCI Express solutions for Servers, Cloud and Storage platforms. He has close to 16 years of experience in developing PCI Express silicones and systems starting PCIe IP cores in IBM design labs based on first drafts of 3GIO (later renamed to PCI Express) spec. During his career Alex has worked in many areas, including InfiniBand, PCIe IPs/Switches, advanced IO virtualization solutions, NextGen switch fabrics and programmable engines for networking packet processing and traffic management.

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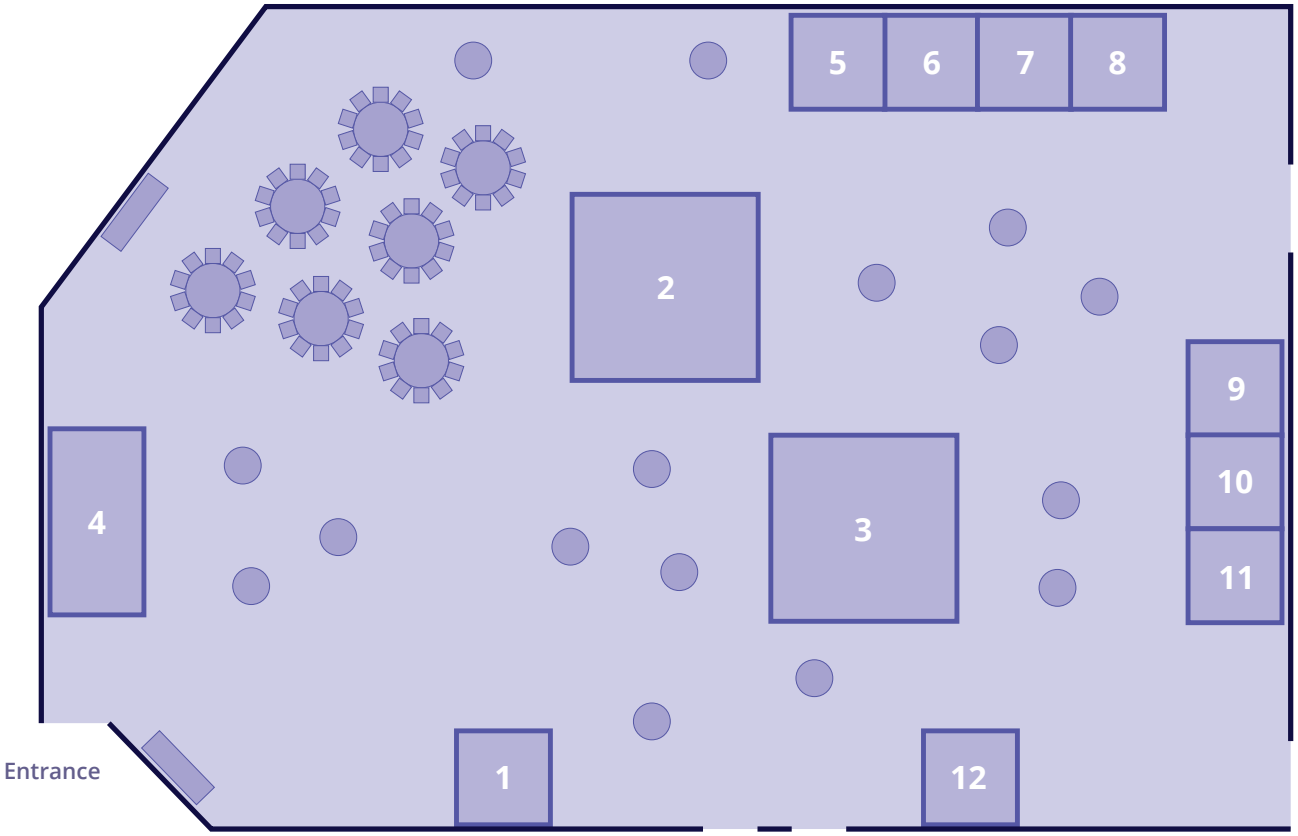
EXHIBIT AREA FLOOR PLAN



Company	Booth #
Avery Design Systems	10
Cadence Design Systems	3
Diodes Incorporated	1
Keysight Technologies	8
Mentor®, A Siemens Business	9
NEC Corporation	7
PLDA	12
Samtec, Inc.	6
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Teledyne LeCroy	4
Viavi Solutions	5

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Avery Design Systems

Avery is a leader in Verification IP providing advanced UVM-based models, compliance test suites, and services for PCI Express, NVMe, CCIX, SATA, UFS/UniPro/M-PHY, USB/xHCI/PD/UAS, SATA, eMMC, SDIO, DDR4/LPDDR3, HBM, HMC, ONFI/Toggle, CSI, DSI, Soundwire, Sensewire, CAN FD, LIN, Flexray, and CHI/ACE/AXI3/AXI4/AHB.

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Mentor®, A Siemens Business, offers a comprehensive PCI Express® verification IP solution that includes SystemVerilog UVM Verification IP (VIP) for fastest time to verification sign-off, and seamless integration into both simulation and emulation environments.

PLDA

PLDA has been successfully delivering PCI Express IP for 20 years. With over 6,000 licenses, PLDA has established the world's broadest PCIe ecosystem and maintained its leadership over four generations of PCI Express specifications, enabling customers to reduce risk and accelerate time to market for their ASIC and FPGA designs.

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